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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,902	10/21/2003	Kazuhisa Suzuki	843.40811VX1	3769

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EXAMINER	
VINH, LAN	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 05/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,902	SUZUKI ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-36* is/are allowed.

6)☒ Claim(s) *1-4 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *102103*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Anand (US 6,362,528)

Anand discloses a method for manufacturing a semiconductor device. The method comprises the steps of:

forming a semiconductor device having a plurality of wiring layers and including a first wiring layer 17b which is not the uppermost layer among said plurality of wiring layers and a second wiring layer 20b higher than said first wiring layer in said plurality of wiring layers (col 10, lines 20-46; fig. 7)

forming an interlayer dielectric film 27 for covering said first wiring layer and forming holes in said interlayer dielectric film on said wiring layer comprising said first wiring layer (col 10, lines 35-36; fig. 7)

forming a mask film 22 for covering at least some of the holes (col 10, lines 64-65; fig. 20)

etching under presence of said mask film (col 6, lines 40-45)

removing an insulating film 29 formed on said interlayer dielectric film including bottoms or insides of said holes (col 13, lines 58-61; fig. 43)

removing said mask film and forming a conductive member 28 on insides of said holes (col 13, lines 57-59; col 14, lines 5-10; fig. 43-44)

Regarding claim 2, Anand discloses the step of formed the insulating film 29 on an entire surface of said interlayer dielectric film including insides of said holes after forming said holes of said interlayer dielectric film (fig. 39)

Regarding claims 3-4, Anand discloses the step of forming wiring layer 28/conductive member connected with wiring 21 (col 14, lines 8-10)

3. Claim 37 is rejected under 35 U.S.C. 102(e) as being anticipated by Matumoto (US 6,165,899)

Matumoto discloses a method for manufacturing a semiconductor device having a plurality of wiring layers and including a first wiring layer 202 which is not the uppermost layer among said plurality of wiring layers and a second wiring layer 209 higher than said first wiring layer in said plurality of wiring layers (col 6, lines 19-20; col 7, lines 7-9; fig. 5F). The method comprises the step of:

determining a via plug area /an intersectional area where a first power-source wiring to which a first voltage/potential is assigned among power source wiring comprising said wiring layer intersects a second power-source wiring to which a second potential difference is assigned (col 7, lines 15-27)

forming a trench/hole in the via plug area/ intersectional area (col 6, lines 64-66)

widening the width of the trench/hole pattern so as not to reach the wiring areas of the first ann second wiring adjacent to the trench/hole pattern (fig. 5F)

Allowable Subject Matter

4. Claims 5-36 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claims 5, 6, the cited prior art of record , taken alone or in combination, fails to disclose a method for manufacturing a semiconductor device comprises the step of etching the fourth insulating film by using the second mask film or the fifth insulating film as a mask, forming the trenches patterned on said fifth insulating film on said fourth insulating film, etching the second insulating film by using the third insulating film as a mask, and forming the holes patterned on the insulating film on the second insulating film, in combination with the rest of the limitations of claims 5-6.

Regarding claim 7, the cited prior art of record, taken alone or in combination, fails to disclose a method for manufacturing a semiconductor device comprises the step of etching the first insulating film at the bottoms of the holes under presence of the third mask film, in combination with the rest of the limitations of claim 7.

Regarding claim 10, the cited prior art of record, taken alone or in combination, fails to disclose a method for manufacturing a semiconductor device comprises the step of depositing a sixth insulating film on the entire surface of a semiconductor substrate including insides of the holes, in combination with the rest of the limitations of claim 10

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
May 24, 2005